

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

YOR920000660U (13959)

Application Number

09/855,240

Applicant(s)

Louis L. Hsu, et al.

Filing Date

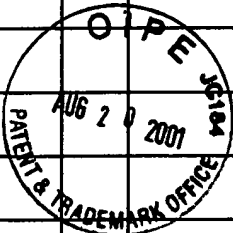
May 15, 2001

Group Art Unit

2818

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE



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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

KAM		Yasuharu Sato, et al., "Fast Cycle RAM (FCRAM); a 20-ns Random Row Access, Pipe-Lined Operating DRAM", <u>IEEE Symposium on VLSI Circuits Digest of Technical Papers</u> , pp. 22-25, June 1998
KAM		Yasuhiro Agata, et al., "An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D2RAM)", <u>IEEE International Solid-State Circuits Conference</u> , pp. 392-393, February 9, 2000

EXAMINER <i>Emily M. Lee - Mayo</i>	DATE CONSIDERED <i>November 22, 2002</i>
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.